



SOLID-STATE OPTICAL LOGIC

Inventor: Jonathan Westphal
7620 Valley Vista Road
Pocatello, Idaho 83201

Citizen of United Kingdom

Prepared By: David L. Stewart
Allen, Dyer, Doppelt, Milbrath &
Gilchrist, L.L.C
255 South Orange Avenue, Suite 1401
P.O. Box 3791
Orlando, FL 32802-3791
Tel: 407-841-2330
Fax: 407-841-2343

SOLID-STATE OPTICAL LOGIC

Inventor: Jonathan Westphal

5

CROSS REFERENCE TO RELATED APPLICATIONS

10 **[0001]** This application is related to and claims priority to provisional patent application 60/438,047, filed January 4, 2003, entitled Solid-State Optical Nor-Gate.

BACKGROUND OF THE INVENTION

15

Field Of The Invention

[0002] The solid-state optical logic described in the application relates to the field of optical signal processing and optical computing, especially in telecommunications applications.

20

Description Of Related Art

25 **[0003]** Attempts to implement a logically complete system of optical processing have had difficulty in the past due to two unsolved problems. The first is the non-linear responses of available optical materials. Unlike silicon logic implementations, the optical AND function has been bedeviled by the linearity of intensity sums: there is no intensity threshold which functions as the analog of a PN device. The second is the inherent

30 difficulty of implementing a NOT function which reverses input 1 to 0 and 0 to 1. It is
simple enough to create a blocking device which on optical 1 input produces a 0 optical
output. But if indeed the optical 1 is the presence of an optical signal, then the optical 0
input must output an optical 1, i.e. the absence of input must result in a positive output.
Thus there is to date no solid-state optical implementation of a complete logic system, i.e
35 an optical NOR or NAND function.

SUMMARY OF THE INVENTION

40 [0004] This invention overcomes a problem of the prior art described above in
that it provides complete set of logical functions, using spatial light modulators or phase
shifters and beamsplitters to produce optical logic and devices for executing logical
functionality.

45

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] The invention will be described more in detail hereinafter by reference to
the following drawings in which:

50

[0006] Figure 1 is an illustration of optical circuitry utilized in carrying out one
aspect of the invention.

55 [0007] Figure 2 represents an improvement on the invention of figure 1 and
which constitutes the best mode known at the moment for carrying out the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0008] As shown in figure 1, a first embodiment of the invention consists of four beamsplitters 110, 115, 120, 125, reflectors 150, 155, 160, 165, 170, 175, and two spatial light modulators (SLMs), 130, 135 or phase modulators. Light enters the device at S, and is split at beamsplitter 110. The two resulting beams are mutually coherent. Light leaving 110 on a easterly track (assuming north points to the top of the page) enters beamsplitter 115). This light is again split into two mutually coherent beams. The reflected beam under goes a phase shift of 180° on reflection. The transmitted beam substantially maintains its phase unchanged. The northerly beam is reflected into Gate 1, the XOR gate, which is beamsplitter 120, passing through an SLM or phase modulator 130. The SLM may be optically or electronically addressed. The SLM or phase modulator selectively reverses the phase of its input beam. The beam exiting 115 in a northerly direction is reflected in to Gate 1, or beamsplitter 120, passing through another SLM (SML2-135) or phase modulator, which selectively reverses the phase of the input, depending on the state of the control signal.

[0009] Turning to the operation of figure 1 in more detail, if control signal 1 is ON at the input phase modulator 1, but control signal 2 is OFF, the result is that the two beams in 120 combine and exit 120 in an easterly direction. The same is true if control signal 1 is OFF and control signal 2 is ON; a single beam exits the beamsplitter in an easterly direction.

[0010] If either control signal 1 and 2 are both ON or both OFF, the result is that the beams input into (c) are mutually coherent, and in both cases a single beam exits (c) in a northerly direction.

[0011] Thus the output from the east port of 120 is a logical XOR function. It is ON or 1 iff the input pattern of the two control signals is 10 or 01, otherwise OFF or 0.

90 [0012] The output from the north port of (c) is a logical COIN function. It is ON or 1 iff the input pattern of the two control signals is 11 or 00, otherwise OFF or 0. This means that whenever the two input beams carry the *same* or coincident (COIN) logic information, or are physically in phase, the output in the north port of (c) is 1.

95 [0013] The purpose of the next optical logic operations in the device is to distinguish the two forms of the northerly COIN output from 120. This COIN output enters gate (2) or beamsplitter 125 and is combined with the half the original input from S, proceeding via 110. If the SLMs or phase modulators have no input from the control signals and register the input pattern 00, then the COIN outputs combine with the original
100 northerly output from 110 and thus from S. The result is that the beams combine in 125 and exit north, giving a NOR output. This can be used as a new control signal.

[0014] If on the other hand the control signals into Gate 1, the beamsplitter 120, are both ON, then the COIN beam entering 125 is exactly out of phase with the beam
105 entering 125 from 110 and S. In that case the two beams input into 125 combine and exit in an easterly direction. This beam is ON iff both SLMs or phase modulators in 120 are ON; it produces an AND output. There is a beam exiting north from 125 iff both inputs in to 120 are OFF, i.e. if the phases of the beams into 120 are undisturbed and the same as those entering 125 from S via 110. The northerly output of 125 is ON iff both control
110 signals are OFF. The northerly 125 output is thus the desired NOR function.

[0015] The function of the destructive interference at the reflector 175 leading into the west port of 125 is to prevent light from S entering 125 when the XOR output of 120 is ON, i.e. when the COIN output of 125 is supposed to be OFF. There must be a
115 destructive interference of the unwanted S beam by the XOR output from 120 when the COIN function is in the OFF or 0 state.

[0016] All other logical functions can be constructed from the NOR elements, and thus all computable functions can be computed by arrays of the NOR-gate described. In
120 this respect the described NOR-gate is the optical equivalent of the silicon AND or NOR

gates. It consists only of optical components, and can be operated without ensuring mutually coherent light sources, as there is a single source S. The final output beam at the NOR OUTPUT derives from S in an unimpeded run through the device. The only speed limitation on a positive throughput signal is the speed with which the light travels through the device down the two arms from S to the NOR OUTPUT.

[0017] Figure 2 of the drawings represents an improved version of the invention shown in figure 1. When working with the invention as described in figure 1, it became apparent that one could not achieve extinction of the beams as completely as one might desire in particularly in the destructive interference process occurring at a reflector 175 of figure 1. Figure 2 represents an improved configuration over that shown in figure 1, which results in improved extinction and improved signal quality over that shown in figure 1.

[0018] Beamsplitters 110 and 115, reflector 150, spatial light modulators 130, 135, reflector 155 and beamsplitter 125 function substantially is outlined in conjunction with figure 1. A phase shifter 200, is placed in the path of the light beam exiting beamsplitter 110 on a northerly direction and the subsequent reflector 210. Beamsplitters 120 (a) labeled XOR and 120 (b) labeled COIN provide the functionality associated with beamsplitter 120 in the embodiment shown in figure 1.

[0019] The embodiment shown in figure 2 differs from that in figure 1 in that separate beamsplitters are utilized to generate the XOR output and the COIN output. This allows a certain parallelism that permits more complete cancellation of signals over the configuration shown in figure 1. The respective XOR and COIN outputs are combined in beamsplitter 125 (after the XOR output passes through beamsplitter 220) to produce a NOR output on the easterly output of beamsplitter 125 and to produce an AND output on the northerly output of beamsplitter 125.

150 **[0020]** This embodiment is preferred because it requires less adjustment of reflectors and achieves more complete cancellation of light beams resulting in cleaner output signals, and balances the power on both arms of the interferometric paths.

155 **[0021]** Using the techniques described herein one can generate a complete set of optical devices that can be utilized to implement completely optical logic which can be utilized in a wide array of devices. For example, logic for computer systems can be enhanced and hardened against certain types of interference utilizing the optical devices described herein. Communication devices, interfaces and circuits can also be generated utilizing the techniques described herein. The result will be faster and more reliable on
160 computers, processors and communication devices.

[0022] The optical device of figure 2 uses wave retardation and beamsplitters to create a NOR-gate.

165 **[0023]** Let two orthogonal and mutually coherent beams enter a beamsplitter 120A from the west (W) and from the south (S) representing respectively vectors p and q . The axis of the beamsplitter is orthogonal to the XOR, or $p\bar{q} \vee \bar{p}q$, axis. The two possible outputs are XOR and its dual COIN.

170 **[0024]** If one of the two input beams is delayed by a phase shifter, or for parallel operations a spatital light modulator (SLM), activated by an optical or electronic control signal, then one of the possible outputs beams [say to the north (N)] will possess an XOR functionality.

175 **[0025]** If both or neither beams are delayed, we have the dual COIN output, traveling east from 120A.

[0026] The truth-table for the COIN function is:

p	q	pCOINq
T	T	T
T	F	F
F	T	F
F	F	T

[0027] We notice that the vector $pq \vee \overline{pq}$ would be equivalent to $\overline{p} \overline{q}$ if we could delete the disjunct pq . In figure 1 we achieve this result optically by bringing the COIN output from beamsplitter 120 as input, with the second input into 125 being a reference beam from the original source. The light exiting beamsplitter 125 east (E) is ON if and only if the two control signals on beamsplitter A are OFF.

[0028] Although the exemplary embodiments have been disclosed herein, the scope of the invention is not limited thereto but rather is expressed in the claims set forth hereinafter.